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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/556,398

11/10/2005

Francois Droz

90500-000067/US

6278

30593

7590

11/24/2010

HARNESS, DICKEY & PIERCE, P.L.C.

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EXAMINER

MAI, THIEN T

ART UNIT

PAPER NUMBER

2887

MAIL DATE

DELIVERY MODE

11/24/2010

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/556,398	<b>Applicant(s)</b> DROZ, FRANCOIS	
	<b>Examiner</b> THIEN T. MAI	<b>Art Unit</b> 2887	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 24 February 2010.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1,2,6 and 9-21 is/are pending in the application.
- 4a) Of the above claim(s) 15-21 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,6 and 9 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 November 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

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**DETAILED ACTION**

***Continued Examination Under 37 CFR 1.114***

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2/24/2010 has been entered.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1-2, 6, 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over EP 1 544 787 A1 (*Reignoux* hereinafter)

Re claim 1, *Reignoux* discloses a process for assembling at least one electronic component made up of a chip provided with contacts on one of the faces of the chip, said contacts being set off on a conductive film constituting flat conductive areas that extend the contacts of the chip in a plane over the chip, the conductive areas being connected to conductive tracks placed on a surface of a planar insulating substrate, comprising:

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- placing the substrate on a work surface, the face including conductive tracks (i.e. antenna pads 31, 41) being oriented upwards (Figs. 1-9),

- placing the electronic component (i.e. module 43 with chip 48) into a cavity of the substrate situated in a zone including the conductive tracks, the chip being inserted into the cavity, the conductive areas of the electronic component coming into contact with the corresponding conductive tracks of the substrate (Figs. 1-9), and

- forming a layer of insulating material (i.e. overlay 49 shown in Fig. 4) which extends concurrently on the electronic component and at least on the zone of the substrate surrounding said electronic component, wherein the conductive areas of the electronic component and the conductive tracks of the substrate are in contact to achieve an electric connection via a pressure of application of the insulating material layer on the electronic component, and after forming the layer of insulating material, the contacted conductive areas of the electronic component and the conductive tracks of the substrate are configured to touch together when repeated stresses are exerted on the substrate.

*Reignoux* is silent to the conductive areas and the tracks rub together.

However, it would have been obvious to one of ordinary skill in the art at the time the invention was made that they rub together due to available space surrounding the electronic component and/or chip and/or overlay when repeated squeezing of the card.

Re claim 2, the electronic component is coated by an insulating material (i.e. glue -paragraph 21) on the face of the chip opposite to the face provided with contacts.

Re claim 6, the cavity is obtained by heating the chip of the electronic component (paragraphs 11, 19, 24 describe the chip is embedded in a resin; it would have been obvious to one of ordinary skill in the art at the time the invention was made that the chip is heated through the hot resin during embedding in order for the chip to stay embedded), then pressing said chip into the substrate material so that the conductive areas of said electronic component are applied against the surface of the substrate (Fig. 4 and 5 show pressure is applied to both sides of the card).

Re claim 9, the cavity is formed by milling or by stamping a window (Figs. 1-9).

***Election/Restrictions***

1. Newly submitted claims 15-21 are directed to inventions that are independent or distinct from the invention originally claimed for the following reasons: Claims 15-18 are directed to a method comprising the steps of “placing a first substrate on a work surface, placing the chip of the electronic component into a cavity of the first substrate, the conductive areas of the electronic component being applied against the surface of the first substrate, and assembling the first substrate provided with the electronic component on a second substrate provided with conductive tracks, so that the conductive areas of the electronic component applied against the surface of the first substrate connect to the conductive tracks of the second substrate, wherein the conductive areas of the electronic component and the conductive tracks of the second substrate are in contact to achieve an electric connection via a pressure of application of the second substrate on the electronic component, and configured to rub together when repeated stresses are exerted on the substrates”. This method is distinct from the invention originally claimed.

Furthermore, claims 19-21 are directed to another method comprising the steps of “placing a first substrate on a work surface, placing the chip of the electronic component into a cavity provided with a window cut into a first substrate with a thickness approximately equal to that of the module, the set of fiat contacts shows on the surface level of said first substrate, and assembling the first substrate provided with the electronic component on a second substrate provided with conductive tracks, so that the conductive areas of the opposite face of the electronic component connect to the conductive tracks of the second substrate, wherein the conductive areas of the electronic component and the conductive tracks of the second substrate are in contact to achieve an electric connection via a pressure of application of the second substrate on the electronic component, and configured to rub together when repeated stresses are exerted on the substrates”. This method is also distinct from the invention originally claimed.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits.

Accordingly, claims 15-21 are withdrawn from consideration as being directed to a non-elected invention.

See 37 CFR 1.142(b) and MPEP § 821.03.

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***Remarks***

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Applicant's request for examination of withdrawn claims 15-21 is respectfully denied since in accordance with 37 CFR 1.142(b) and MPEP § 821.03, they are directed to inventions independent and distinct from the original invention that has been examined on the merits.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to THIEN T. MAI whose telephone number is (571)272-8283. The examiner can normally be reached on Monday through Friday, 8:00 - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steve S. Paik can be reached on 571-272-2404. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Thien T Mai/

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